

FIG. 1

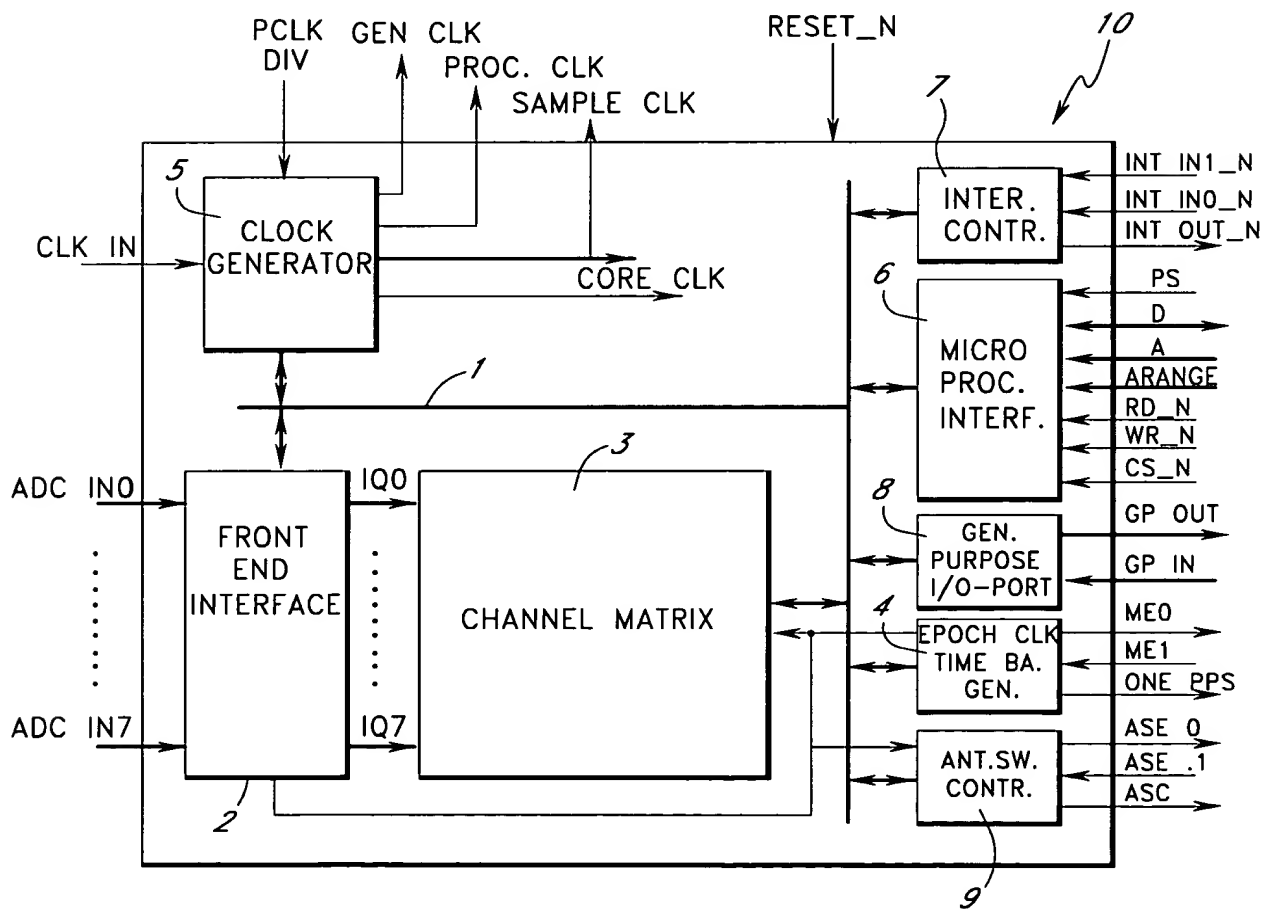


FIG. 2

FIG. 4

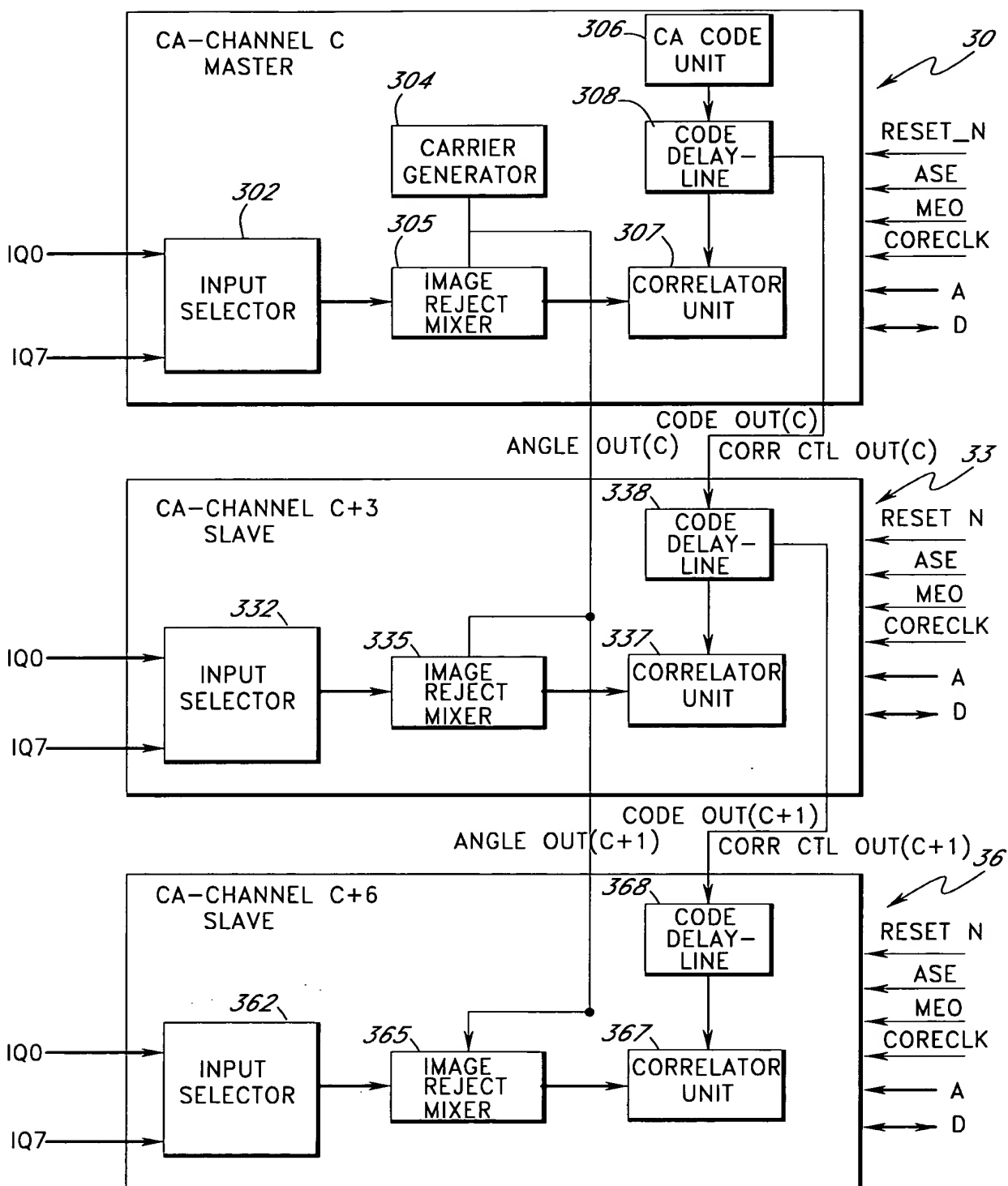


FIG.5



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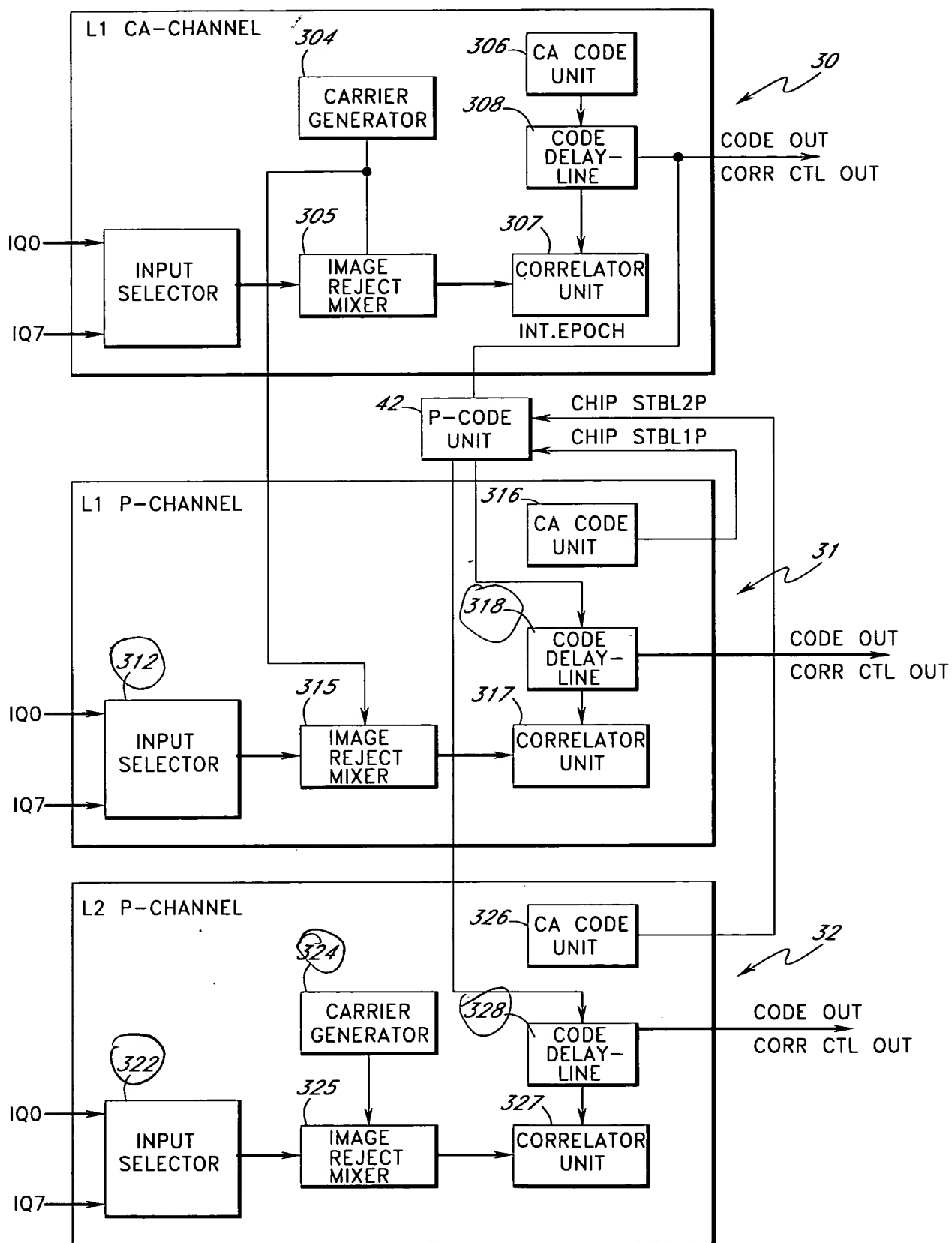
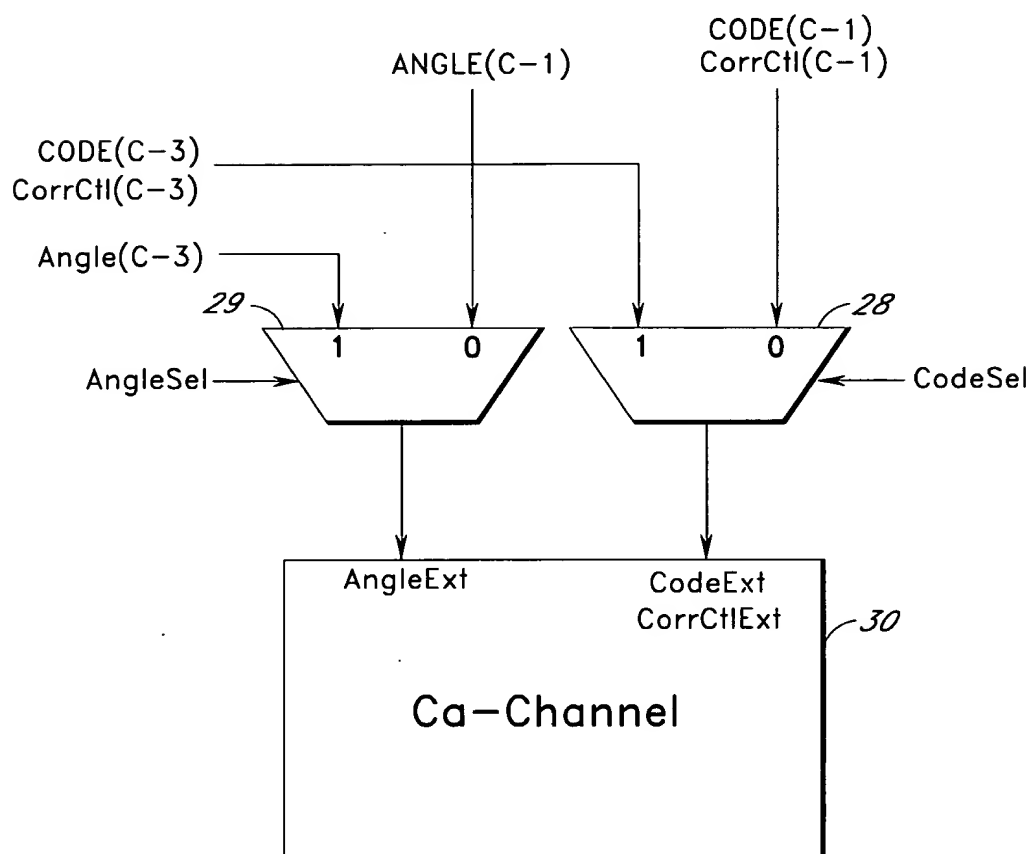
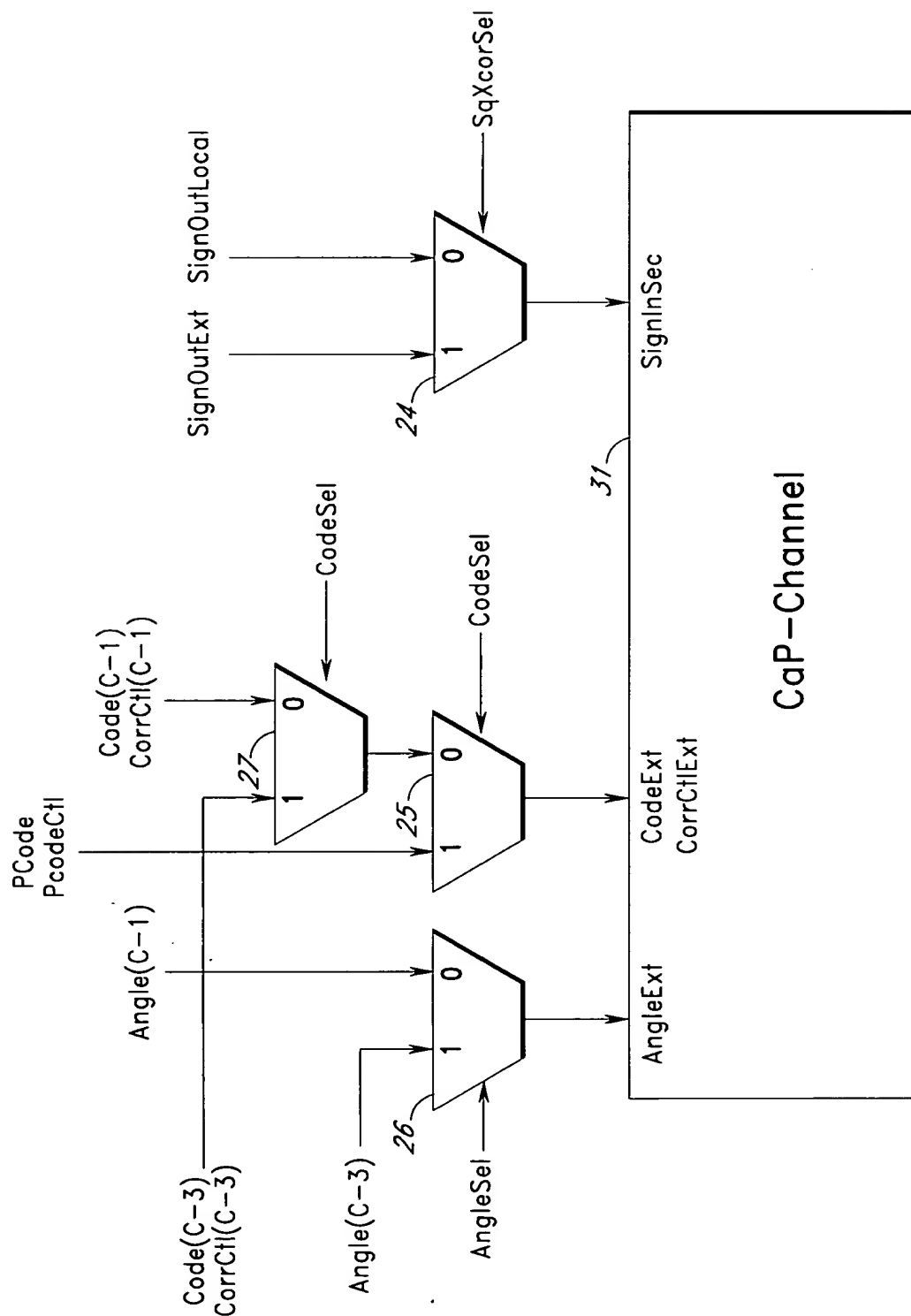


FIG. 6



A)

FIG. 7A



B)

FIG. 7B

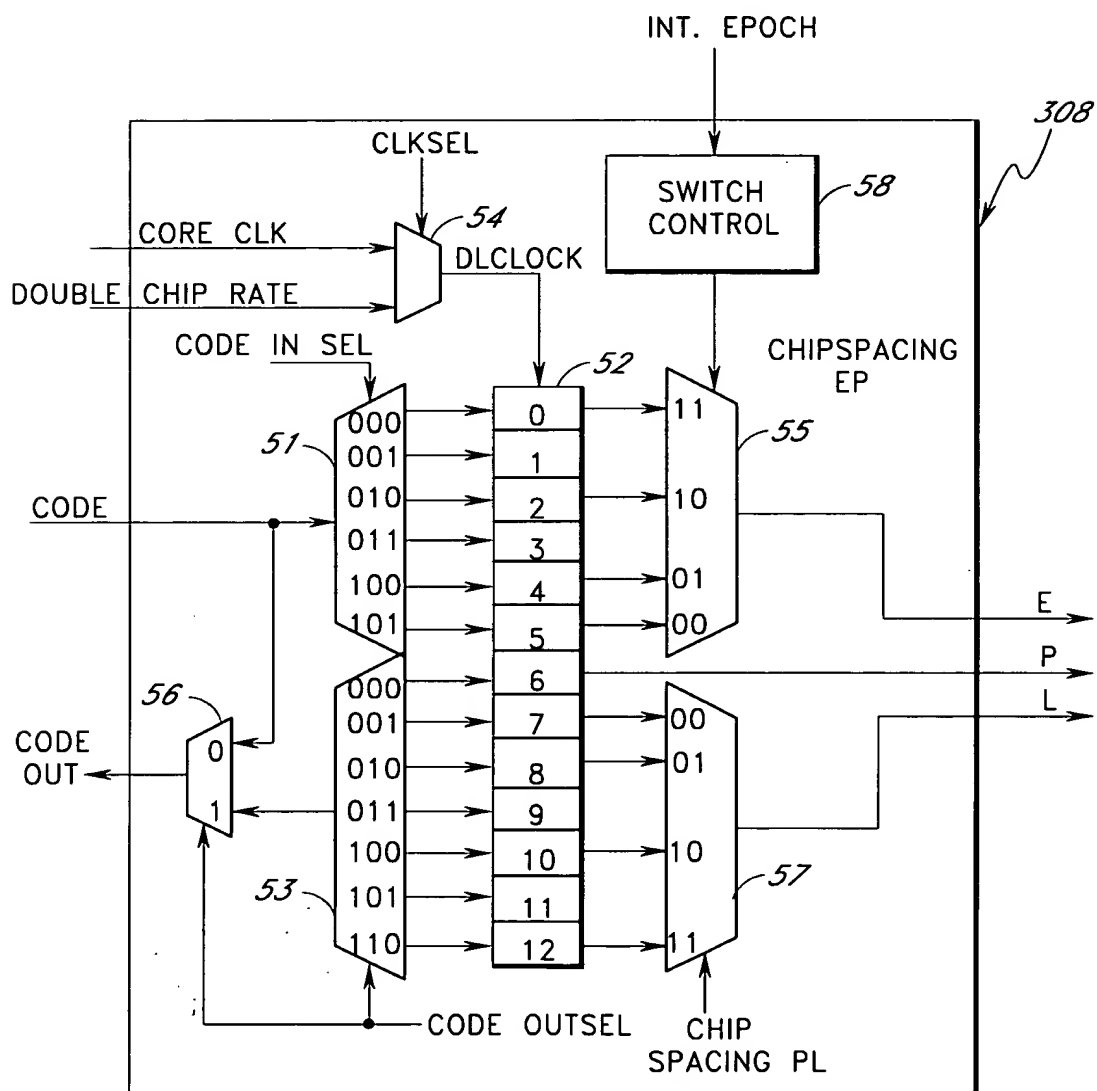
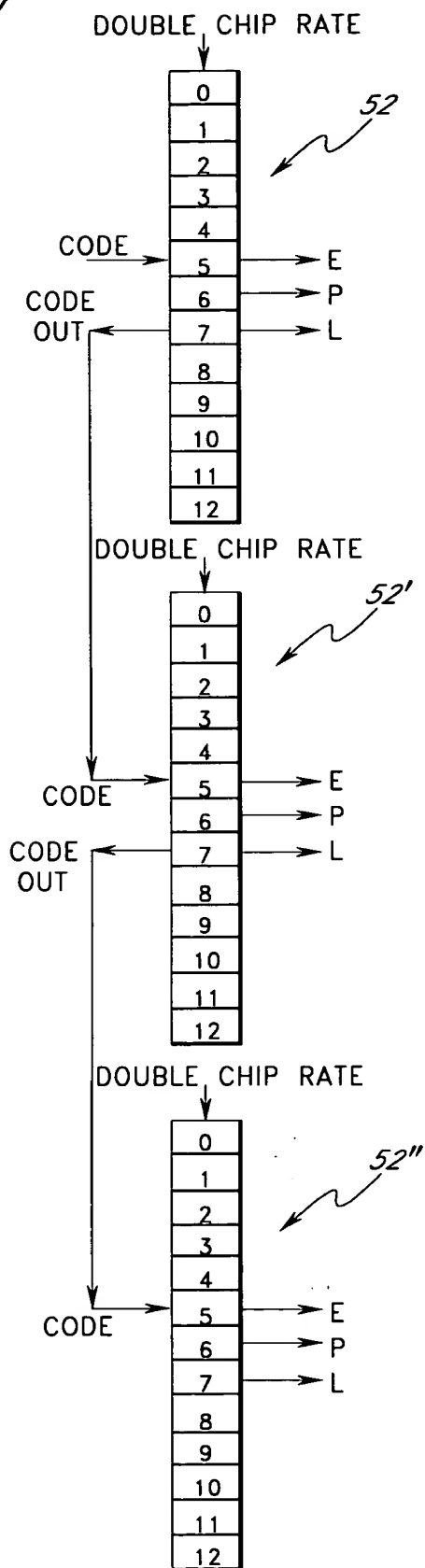


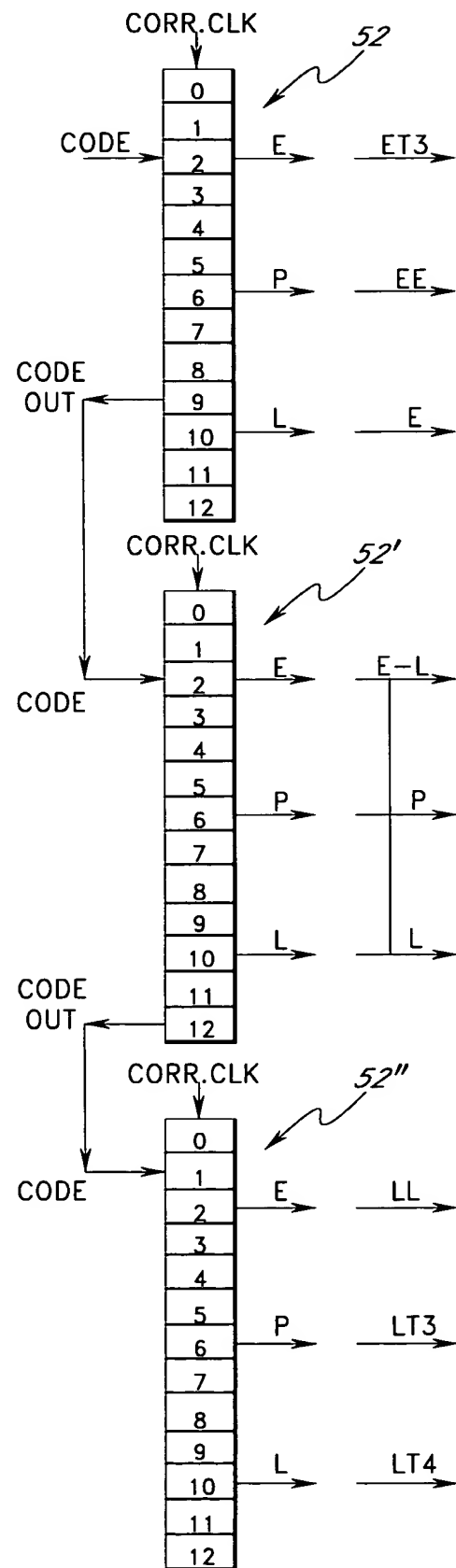
FIG. 8



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(A) FAST ACQUISITION MODE

FIG. 9A

(B) MULTIPATH MITIGATION WITH 8T SPACING BETWEEN E AND L

FIG. 9B

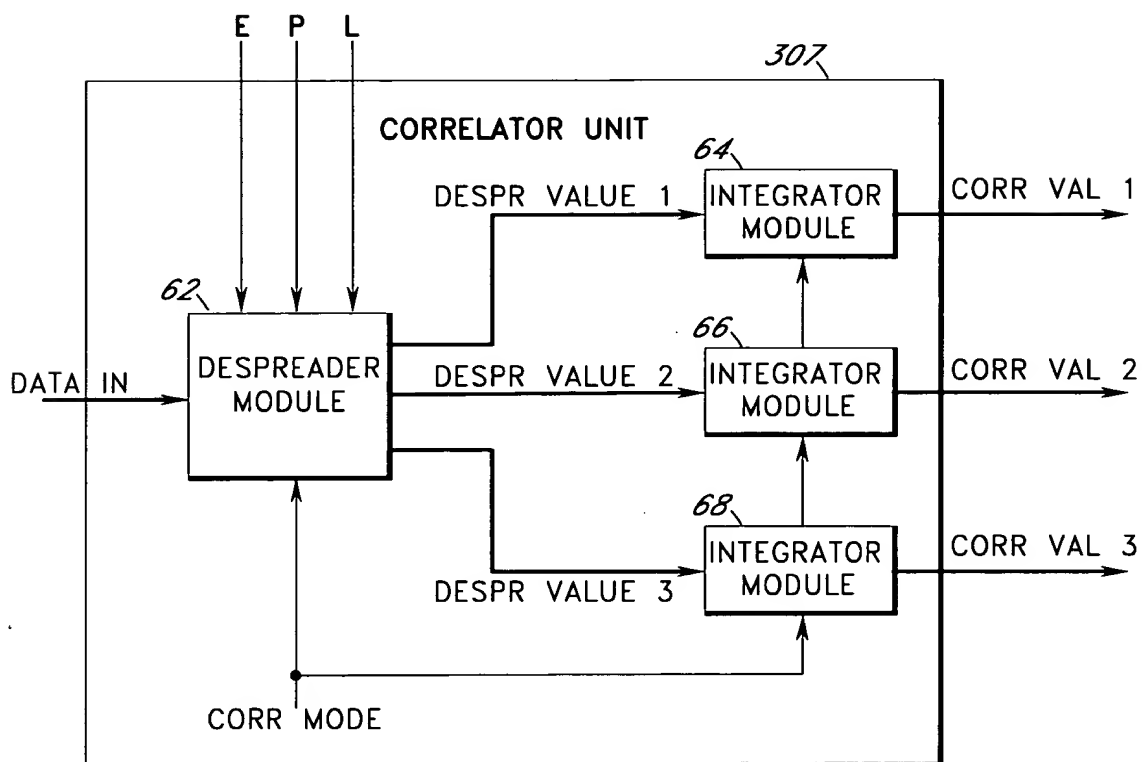


FIG. 10

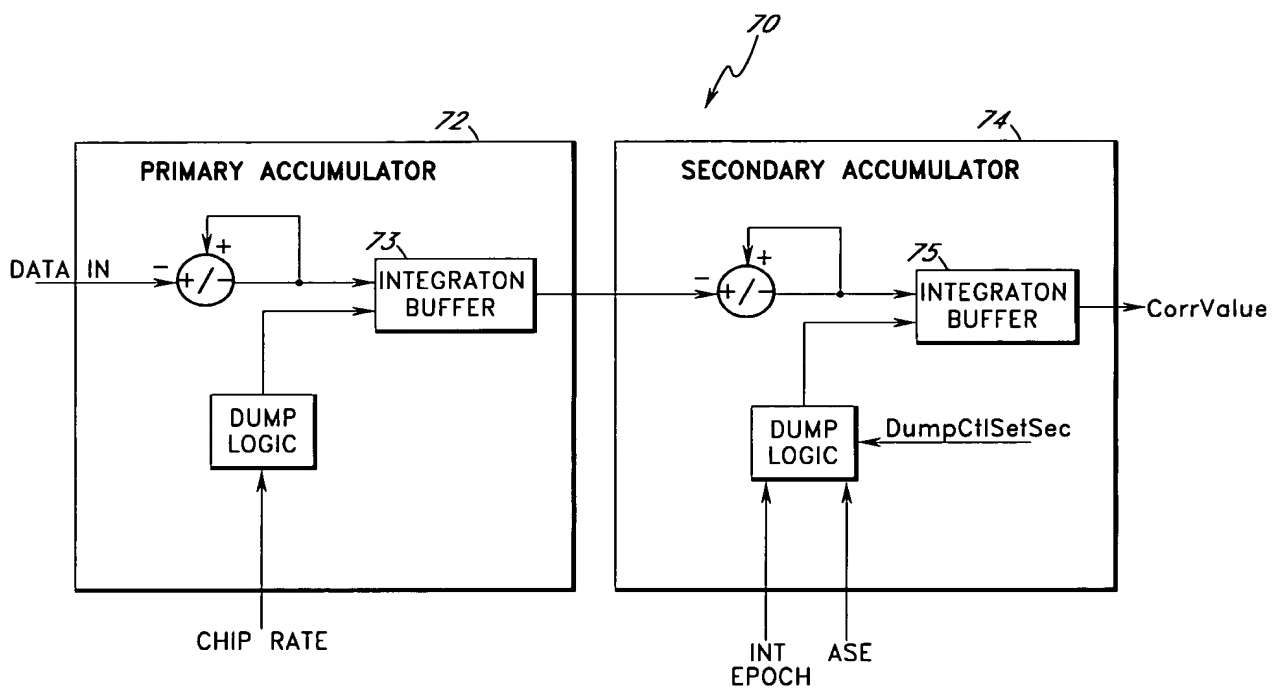


FIG. 11

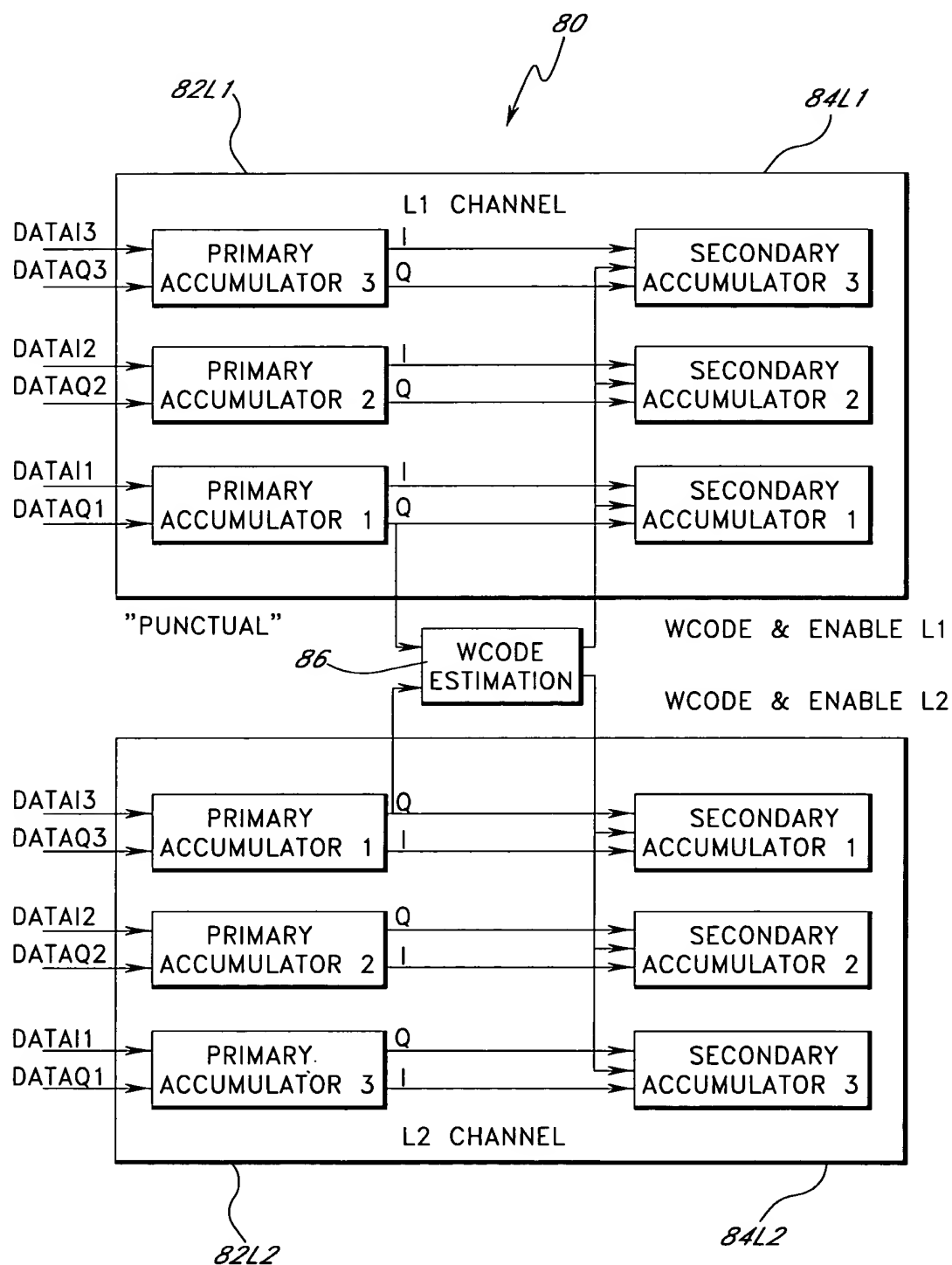


FIG. 13

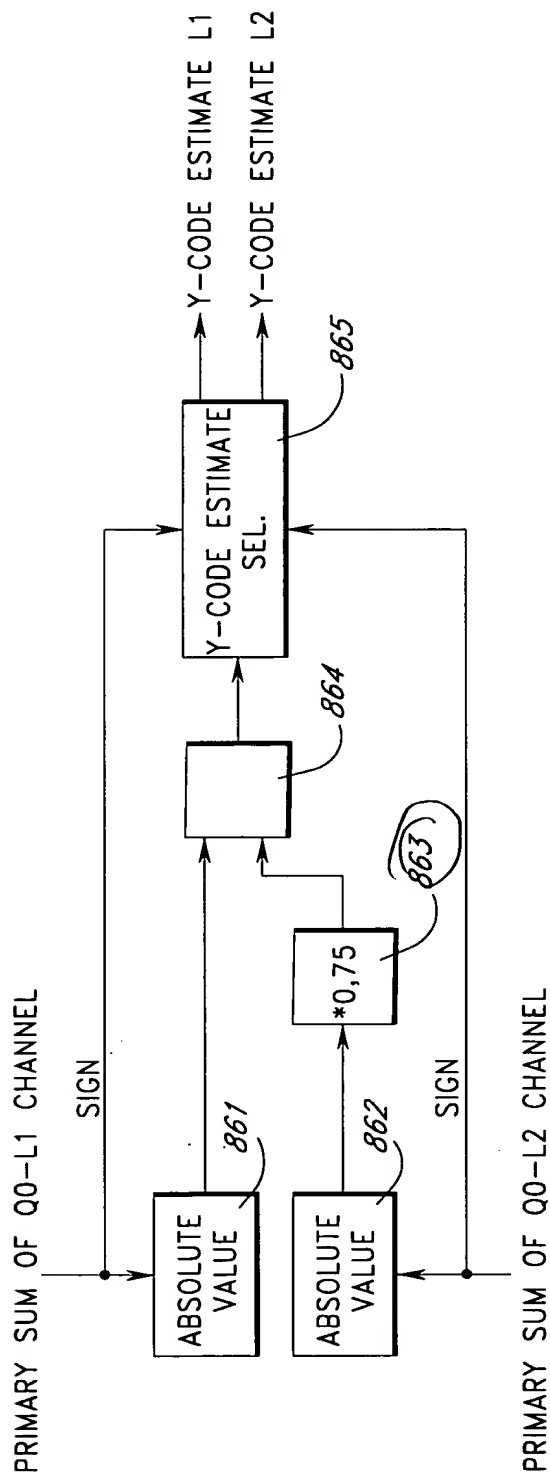


FIG. 14

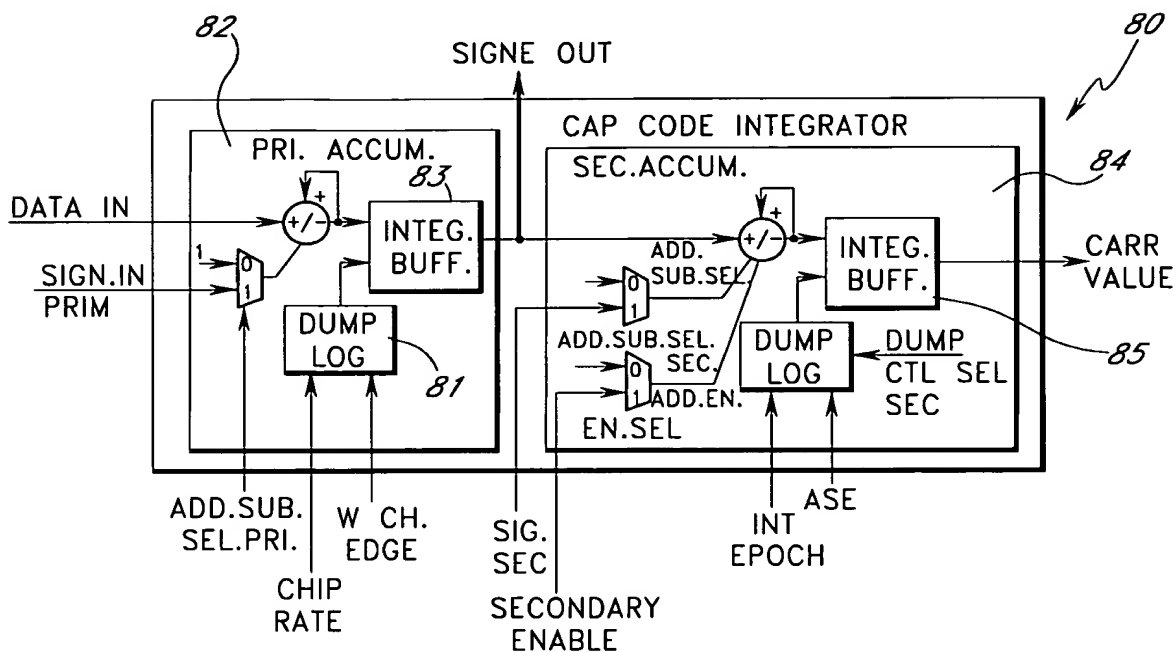


FIG. 12

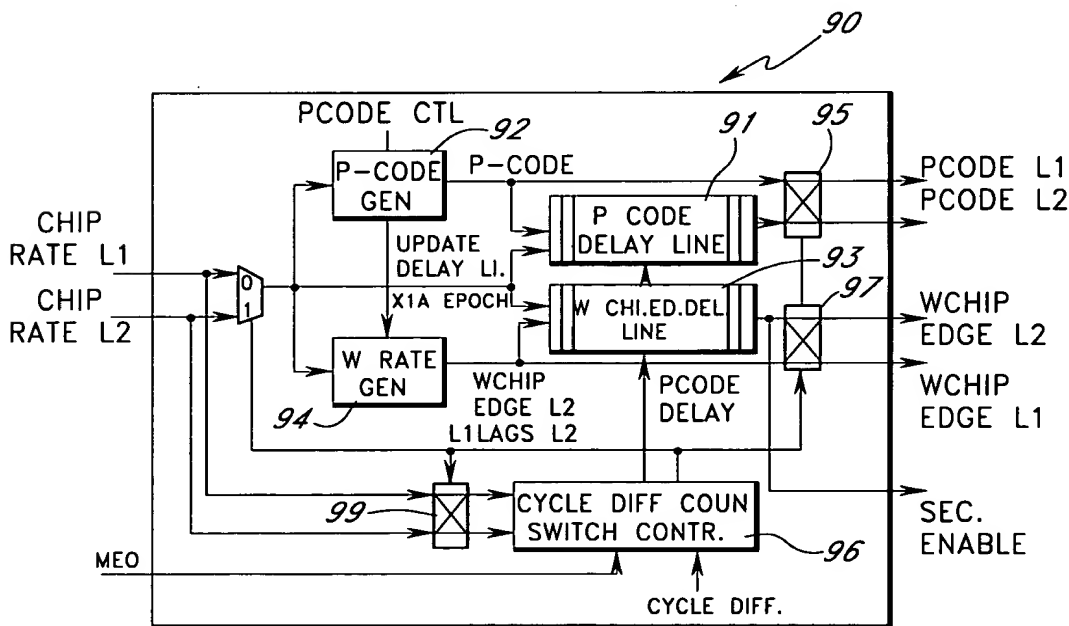


FIG. 15